## **Getting Started with Altera Quartus II**

**NOTE:** Step 1 and Step 2 are to be followed only if you are installing Altera Quartus II for the first time. If you are using EECS commons or lab computers, you can start with Step 3 as the software is pre-installed.

#### Step 1: Install the Altera Quartus 7.1 CD that comes with your book

1.) The Quartus II CAD software can be installed by running the following command in the command prompt: **Start->Programs->Accesories->Command** 

#### <CD-ROM drive>:\CDROM\Quartus\_II\72sp2\_quartus\_free.exe

(For my computer the CD-ROM drive was H:)

2.) The installation process involves a series of steps. Choosing a complete install will require approximately 1.5 GB of free space. Make sure you have enough space on your target directory.

#### Step 2: Obtaining the license file

1.) After the installation you need a license file which has to be downloaded.

- 2.) Open your browser and go to www.altera.com/licensing
- 3.) Click on the Get licenses link which is the first blue link on the page

# 4.) Click on Get a license for Quartus® II Web Edition software and the ModelSim®-Altera Web Edition software that is also the first link on the page

5.) You should create an account using your e-mail address. Alternatively, you can use the **Get one time access** option. You will be asked to enter information about you in this process.

6.) Once you have an username and password you can go back to Step 2.5 and now enter the username and password.

7.) As part of the procedure you will be asked to provide your network interface card number.

The Network Interface Card (NIC) number is a 12-digit hexadecimal number that identifies your computer. You can find the NIC number for your network card by typing **ipconfig** /all at a command prompt. Your NIC number is the number on the physical address line, minus the dashes, for example, 00C04FA392EF

So, to obtain this number, type the following command in a Windows Command Prompt window: ipconfig /all

Look for the line of the form

The last part of this line is the network interface card number. In this example, you would type 00C04FA392EF (without the - dashes) into the box that says "Enter your network interface card (NIC) number:" on the licensing web page.

Once you have provided to Altera the required information to obtain your license file, the file will be emailed to you along with instructions on using the license file. The email is normally returned to you from Altera in less than one hour. (Reference: README file of the Altera Quartus 7.1 CD)

8.) The instructions to download and specify the license file to Altera will be given to you in your email which has the license file

#### **Step:3 Creating a New Project**

#### Let us design, compile and simulate a simple three input AND gate:

1.) After obtaining the license you can start working on Quartus by creating a project. Go to **File**>**Create New Project wizard** 

2.) In the window that pops up you have to enter the directory where you want to store your project files, the file name and a project name and click **Next**. (Note: The file name should be the same as your top-level entity). This is shown in Fig. 1

New Project Wizard: Directory, Name , Top-Level Entity [page 1 of 5]	×
What is the working directory for this project?	
E:\Altera\quartus\My Altera Work\first_vhdl_andgate	
What is the name of this project?	
andgate	
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.	
andgate	
Use Existing Project Settings	
< Back Next > Finish Cancel	

Fig. 1. New Project Wizard

3.) In this step you will be asked to enter the family and device settings. You need not worry about this step if you are not downloading your design to a board. Click **Next**.

4.) Next is the EDA Tools Settings. You need not worry about this step if your project does not depend upon files from other projects. Click **Finish**. The final screen should be something like Fig.2. It might look somewhat different for you but you can ignore the device assignment settings. Just make sure that your project directory and file name are the same as you had entered. Click **Finish** once you are done.

New Project Wizard: Summa	ry [page 5 of 5]	×
When you click Finish, the projec	t will be created with the following settings:	
Project directory:		
E:/Altera/quartus/My Altera \	Work/first_vhdl_andgate/	
Project name:	andgate	
Top-level design entity:	andgate	
Number of files added:	0	
Number of user libraries added:	0	
Device assignments:		
Family name:	FLEX10K	
Device:	EPF10K70RC240-4	
EDA tools:		
Design entry/synthesis:	<none></none>	
Simulation:	<none></none>	
Timing analysis:	<none></none>	
	< Back Next > Finish Cancel	

Fig 2. Summary of the New Project Wizard

5.) After creating a new project you can create the VHDL design file from **File->New-> VHDL file.** This is shown in Fig. 3

New	×
Device Design Files Other Files AHDL File Block Diagram/Schematic File EDIF File SOPC Builder System Verilog HDL File VHDL File	
OK Cancel	

#### Fig.3 New VHDL file

6.) Save the file into the directory which you specified while creating your project from **File->Saves** As with a .vhd extension Note: By default it will save to your project directory with .vhd extension; you just have to make sure it does. The screen should like the one shown in Fig.4.

Save As					
Save in:	irst_vhdl_and	gate	•	+ 🗈 💣 🔳	•
My Recent Documents Desktop My Documents My Computer	<b>i d</b> b				
My Network Places	File name: Save as type:	andgate VHDL File (*.vhd;*.vho I✓ Add file to current p	dl) project	•	Save Cancel

Fig.4 Save the VHDL file

7.) Now you can start entering your VHDL design. Refer the VHDL tutorial for the design entry. Once you complete your design you can save it from (**File->Save**) or **Ctrl+s** is the shortcut. The AND gate design entry is shown in Fig.5. Note that the entity name is the same as the file name.

🖏 Quartus II - E:/Altera/quartus/My Alt	era Work/fi	rst_vhdl_andgate/andgate - andgate - [andgate.vhd]
🎨 File Edit View Project Assignments Pro	ocessing Tool	ls Window Help
🗅 🖻 🖬 🕌 👗 🖻 🛍 🗠 🗠	- 🔀 🖉 🥙 🐨 🕨 🕫 🗞 🔞 😓 😣 粒 💿	
Project Navigator	👳 andg	ate.vhd
Entity         ▲         FLEX10K: EPF10K70R         ▲         andgate             ▲             Files <b>e</b> <sup>®</sup> Design Units    Status          ▲ <b>Module</b> Progress % Time ③	₩ ₩ ¢ ¢ % 0 2 	<pre>1 LIBRARY IEEE; 2 USE IEEE.STD_LOGIC_1164.ALL; 3 4 entity andgate is 5 port ( x1,x2,x3 : IN STD_LOGIC; 6 f : OUT STD_LOGIC); 7 end andgate; 9 9 Architecture behavior of andgate is 10 begin 11 f &lt;= x1 AND x2 AND x3; 12 end behavior;</pre>

Fig. 5. AND gate design entry

8.) There are pre-defined templates which can be obtained from **Insert->Templates->VHDL for templates**. These templates can help you with the design process.

#### **Step 4 Compiling your design**

1.) Once you have completed your design you should compile it to check for errors.

2.) You can compile it using **Processing->Start->Start Analysis and Synthesis** or **Ctrl+k** is the shortcut for that. This is shown in Fig 6.



Fig.6. Compiling your design

3.) This gives a compilation report. If you get an error you can get more information about the error by selecting the error and pressing F1. This can help you with your debugging process. This is shown in Fig.7



**Fig.7 Compilation Report** 

#### **Step 5: Simulation**

1.) Once you successfully compile your design you can simulate the waveforms.

2.) Click on **File->New->Other Files->Vector Waveform Files** to get a waveform editor window as shown in Fig.8.



#### **Fig.8 Waveform Editor**

You should save it in the same directory with a .vwf extension. Note: By default it will save to your project directory with .vhd extension; you just have to make sure it does.

3.) You can specify the end time for the simulated waveform by specifying **Edit->End time.** This is shown in Fig. 9.

End Time				
Time: 10	us 💌	]		
Default extension opt	ions:			
Extension value: La	ist clock patte	ern 🔽	]	
End time extension pe	er signal:			
Signal Name	Direction	Radix	Extension value	$\Box$
				ncel

Fig 9. Specify End Time

4.) Select View->Fit in Window, to show entire output for the simulated waveform.

5.) Enter the Input and Output Nodes of the circuit from **Edit->Insert Node or Bus**. Click on **Node Finder** from the menu. You should get a window as shown in Fig. 10.

Node Finder				
Named:	Filter: Pins: all	Customize		ок
Look in: landgate		✓ … ✓ Include subentities	Stop	Cancel
Nodes Found:		Selected Nodes:		
Name	Assignments T	Name	Assignments T	
	>			
	>>			
	<u>&lt;</u>			
	<<			
<		<	>	

Fig 10. Node Finder Window

6.) In the resulting window select **all** for Pins from the drop down menu and click on list.

7.) Now all the pins of your design will be listed on the left pane. Select each pin and click on > to move the pin to the right pane. You should repeat this for each pin. Click **OK**.

8.) Now you should be able to get all the pins in your waveform editor window. The screen should look like the one in Fig. 11.

Node Finder				
Named: ×	Filter: Pins: all	Customize	List	ОК
Look in: Iandgate		▼ ▼ Include subentities	Stop	Cancel
Nodes Found:		Selected Nodes:		
Name	Assignments T	Name	Assignments T	
I I I I I I I I I I I I I I I I I I I	Unassigned C	🐵 landgatelf	Unassigned O	
I → ×1	Unassigned Ir	🗩 landgate x1	Unassigned Ir	
■ x2	Unassigned Ir	Implandgate x2	Unassigned Ir	
₩ ×3	Unassigned It	Im landgate x3	Unassigned Ir	
	>>			
	<			
<	>	<	>	

Fig 11. Node Finder

9.) The time period for each waveform (x1, x2 and x3) can be entered by clicking on the **Overwrite Clock** icon from the vertical tool bar in the waveform editor window. This is shown in Fig. 12 and Fig. 13. Let us use a time period of 1, 0.5 and 0.25 microseconds for x1, x2, x3 respectively for this example. Save the input in your project directory with a .vwf extension. After entering the screen should like the one shown in Fig 14. Note the output pin f has does not have a waveform. We will see the output waveform after we simulate.

🐇 Quartus II - E:/Altera/quartus/My Alte	era Work/	/first_v	/hdl_andg	ate/andgat	ie - a	ndgate	- [Wave	eform1	.vwf	ŋ										
File Edit View Project Assignments Pro	ocessing To	ools Wi	indow Help																	
🗋 D 🍃 🖬 🕌 🐇 🛍 💼 🗠 🗠	andgate			- 🎽	{ _	Ø 😻	🔶   4	•	\$	►   •	Ō 👌	: 🕘	۱ 🖉	0						
Project Navigator	🕸 and	lgate.vhc	ł					🕘 (	Compil	ation Repo	ort - Flow S	Summary			🖸	Wavefor	m1.vwf*			
FLEX10K: EPF10K70RC240-4		Master	Time Bar:	15.675	i ns	•	Pointer	:	200.3	25 ns	Interv	val:	184.58 ns	. 9	Start:	0 ps		End:	10.0 u	us
L abd andgate 1 (1)	I A ⊛ A		Name	Value at 15.68 ns	0 ps 15.6	640,0 i 75 ns	ns 1.28	us 1.9	ij2 us	2.56 us	3.2 us	3.84 us	4.48 us	5.12 us	5.76 us	6.4 us	7.04 us	7.68 us	8.32 us	8.9j6
		@0	f v1	AX A D	**	*****	*****	*****	****	*****	*****	*****	******	*****	******	*****	*****	******	*****	****
	<b>纳</b> 公。	2	×2	AO																
	<u>\</u>	₫ 3	×3	AO																
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Status Andule Progress % Time ()	- <u>X2</u> Xe   账 ≵↓	verwrite	Clock																	
		<		>																

Fig 12. Overwrite Clock to enter time period.

С	ock 🛛 🔀
Γ	Time range
	Start time: 0 ps 💌
	End time: 10.0 us 💌
	Base waveform on C Clock settings:
	Time period:
	Period: 1 us 💌
	Offset: 0.0 ns 💌
	Duty cycle (%): 50
	OK Cancel

Fig 13. Enter Time Period



Fig 14. Waveforms

10.) There are two types of Simulator modes: Functional and timing. The difference between them is that functional mode does not show prorogation delays. This can be selected from **Assignment-**>**Settings->Simulator** and choosing Simulator mode. Let us do a functional simulation to start with. The screen should look like Fig 15. Enter the simulation input file by browsing to your project folder. The screen should look like Fig 16.

Settings - andgate	
Settings - andgate Category: General Files Libraries Device Operating Settings and Conditions Compilation Process Settings Compilation Process Settings Compilation Process Settings Fitter Settings Fitter Settings Fitter Settings Simulation Settings Signal Tap II Logic Analyzer Logic Analyzer Interface Simulator Settings Simulation Verification Simulation Output Files PowerPlay Power Analyzer Settings	Simulator Settings         Select simulation options.         Simulation mode:         Timing         Timing         Timing using Fast Timing Model         Simulation period         Image:         End simulation at:         Image:         Glitch filtering options:         Auto         More Settings
	Description:           Specifies the type of simulation to perform for the current Simulation focus.

### **Fig.15 Functional Simulation Settings**

Settings - andgate	_ <u> </u>
Category:  Category:  General  Files  Lubraries  Device  Operating Settings and Conditions  Compilation Process Settings  EDA Tool Settings  Analysis & Synthesis Settings  Filter Settings  Design Assistant  Simulation Strings  Simulation Verification  Simulation Verifica	

Fig. 16 Functional Simulation Settings

11.) Save the changes made till now. If you choose functional mode go to **Processing->Generate Functional Simulation Netlist**. Click OK on the dialog box that appears.

12.) The simulation can be started from **Processing->Start Simulation** or shortcut (**Ctrl+i**). The final output should be like the one shown on Fig.17

The shortcut to compile and simulate is Ctrl+Shift+k.



Fig 17. Simulated Waveform

This ends the tutorial. You can try implementing other designs.