EECS 140
Homework #4
Due April 1, 2008

The objective of this homework is twofold: first to gain experience in creating and testing a circuit using VHDL, and second to examine and compare two common adder circuits. The adder circuits you will be creating and testing are a ripple carry adder and a carry lookahead adder. This assignment will require you to successfully design, compile, and test your adder circuits, so do not wait to get started !

1. Enter and successfully compile the VHDL code given to you in class for the 3-bit ripple carry adder.
2. Simulate the adder to show the correct operation of the adder.
3. Derive the equations for the all sums, generates, propagates and carries for the 3-bit carry lookahead adder (you should have this in your notes)
4. Draw a block diagram of a 3-bit carry lookahead adder showing the 1-bit adders and carry generate blocks with connecting signals (you should have this in your notes).
5. Enter and successfully compile VHDL code for your 3-bit carry lookahead adder.
6. Simulate your adder to show correction operation
7. Comment on the performance between the ripple carry and carry lookahead circuits.